Requested Patent: EP0286412A2

Title: APPARATUS FOR RECORDING AND/OR REPRODUCING DIGITAL DATA ;

Abstracted Patent: EP0286412 ;

Publication Date: 1988-10-12 ;

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Application Number: EP19880303134 19880407 ;

Priority Number(s):

JP19870085388 19870407; JP19870148174 19870615; JP19870158346 19870625; JP19870158885 19870626 ;

IPC Classification: G11B20/10 ; G11B20/12 ; G11B20/18 ;

Equivalents:

AU1434188, AU618729, CA1322243, DE3875773D, DE3875773T, KR133178, US4899232

ABSTRACT:

An apparatus for recording and/or reproducing digital data on a recording medium (12) comprises a recorder (1) similar to a digital audio recorder which records digital signals in frames each made up of two oblique tracks formed by rotary heads (A,B), and a controller (2) for dividing the digital data into predetermined frame portions which can be easily re-recorded, and supplying the divided data to the recorder as a digital signal.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 286 412**
A2

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 88303134.6

(22) Date of filing: 07.04.88

(51) Int. Cl.⁴: G 11 B 20/10
G 11 B 20/12, G 11 B 20/18

(30) Priority: 07.04.87 JP 85388/87
15.06.87 JP 148174/87
25.06.87 JP 158346/87
26.06.87 JP 158885/87

(43) Date of publication of application:
12.10.88 Bulletin 88/41

(84) Designated Contracting States:
AT CH DE FR GB IT LI NL SE

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(54) **Apparatus for recording and/or reproducing digital data.**

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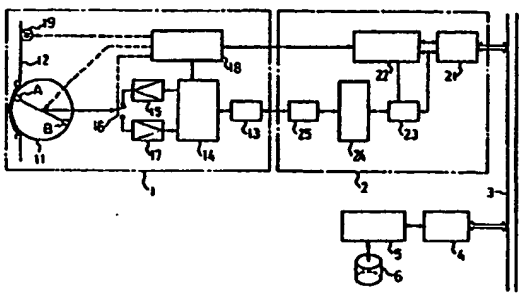
FIG. 1



EP 0 286 412 A2

Description

APPARATUS FOR RECORDING AND/OR REPRODUCING DIGITAL DATA

This invention relates to apparatus for recording and/or reproducing digital data. More particularly, but not exclusively, the invention relates to a rotary head type digital audio tape recorder (R-DAT or DAT) when used for recording data from a computer or the like.

To protect computer generated data written on a hard disc or the like, the data are sometimes transferred to a so-called data streamer (or data recorder) and are thereby recorded (or backed up) on other recording media once per day.

In most cases, a data streamer is what might be called an analogue audio tape recorder. Such a recorder, however, consumes a large quantity of tape. Also, such a data streamer has a low data rate upon recording, so that it takes a long time to transfer and record the data. Moreover, it is not easy with an analogue audio tape recorder to find the starting point of the required recorded data.

When data from, for example, a computer is recorded on an audio tape recorder, an arbitrary file mark signal is supplied thereto from the computer. Upon reproduction, the location number of the file mark for the computer designated address is searched for. Since the recorder is arranged to search for the location number of the file mark by counting the reproduced signal of the file mark in the normal reproduction mode, it takes a long time to search for the required file mark.

A DAT (digital audio tape recorder) has been developed, as described in "ES Review", pages 11 to 14, published December 1985 by Sony Corporation, Shibaura Plant: ISSN 0389-7737. Since this DAT is designed to record and/or reproduce a digital signal, that is a digitized audio signal, it is very suitable for recording the aforesaid data.

However, the width of the DAT recording head is generally larger than the track pitch, so that a portion of the preceding track is erased by the current track, and data is recorded in partially superimposed tracks without a guard band between adjacent tracks. This will cause a problem, for example, when a portion of recorded data is to be reproduced, edited and recorded again. Thus, the reproducing and editing operations can easily be effected, but it is difficult to record the edited data again.

Specifically, when data has been recorded in partially superimposed tracks, if the edited data is re-recorded, the next track in which data has been previously recorded is erased, because the head width of the recording head is larger than the track width. Consequently, data to be retained is destroyed.

To deal with this problem, we have proposed an apparatus which is capable of satisfactorily recording data information by providing an amble signal period at the beginning and end portions of each recording area in which data are recorded at one time using the DAT (Japanese Patent Application No. 61/314922, which corresponds in part with U.S. Patent Application No. 133 010). This apparatus, however, has to re-record all the data recorded in the previous recording operation, so that if there is a large amount of data, a long period of time is necessary for reproducing and recording.

As described above, when a DAT is used as a data recorder, there is the problem that the previously recorded data cannot be easily recorded again.

The data signals recorded by the DAT include an error correcting code such as a Reed-Solomon code. Furthermore, because the DAT is intended to record audio signals, that is a more or less continuous analogue signal, the data errors can be easily compensated for by interpolation techniques, such as previous value holding, even if the error cannot be corrected by the error correcting code.

However, when the DAT is used as a data recorder, data compensation by interpolation techniques such as previous value holding cannot be effected, because of the discontinuous nature of digital data, so that erroneous data can no longer be corrected unless errors are corrected by the error correcting code.

According to the present invention there is provided an apparatus for recording digital data on a recording medium, the apparatus comprising:

recording means for recording an inputted digital signal in one frame, which is made up of two oblique tracks formed by rotary heads;

characterized by:

control means for dividing said digital data into predetermined frame portions and supplying the divided digital data to said recording means.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Figure 1 is a block diagram of an embodiment of recording and/or reproducing apparatus according to the present invention;

Figures 2 and 3A to 3C are diagrams showing an example of a recording pattern on a recording medium made by an embodiment;

Figure 4 is a block diagram of another embodiment;

Figures 5A to 5C and 6 are diagrams showing another example of a recording pattern on a recording medium made by an embodiment;

Figure 7 is a block diagram showing an example of a syndrome generating circuit;

Figures 8A to 8E are timing charts for explaining the operation of reproducing apparatus according to the present invention;

Figure 9 is a diagram showing a DAT format;
Figure 10 shows tables of a recording format of packs in a sub-code area;
Figures 11A and 11B are diagrams showing the identification (ID) organization of a DAT format; and
Figure 12 is a flow chart illustrating a program for generating syndromes for use in error correction.

Referring initially to Figure 1, the data recorder according to a first embodiment of the invention includes a digital audio tape recorder (DAT) 1. The DAT 1 has a rotary head drum 11, and a magnetic tape 12 is wrapped around the peripheral surface of the head drum 11, over an angular range of about 90° of head travel, and is transported past the head drum 11 by a tape transport mechanism 19. Two rotary heads A and B are mounted in the head drum 11, and two oblique tracks are recorded and/or produced by the heads A and B once per revolution of the head drum 11 as shown more clearly in Figure 2.

Incoming digital data is supplied to an input and output (I/O) circuit 13 of the DAT 1. The digital data from the I/O circuit 13 is supplied to a digital signal processor 14, in which it is converted into the DAT format. The digital signal converted in accordance with the DAT format is supplied through a recording amplifier 15 and a recording side contact R of a recording/reproducing change-over switch 16 to the heads A and B, and is thereby recorded on the tape 12.

When the signal recorded on the tape 12 is reproduced by the heads A and B, the reproduced signal is supplied through a reproducing side contact P of the switch 16 and a playback amplifier 17 to the signal processor 14, in which the reproduced signal is reconverted into the digital data and then supplied through the I/O circuit 13 to the outside.

An incoming control signal is also supplied to a system control circuit 18 of the DAT 1. On the basis of the signal from the control circuit 18, the head drum 11 is controlled to rotate, the tape transport mechanism 19 to run the tape 12, and the switch 16 to change in position. Also, upon recording, the signal from the control circuit 18 is supplied to the signal processor 14 which then produces a sub-code signal or the like which will be described later. Upon reproduction, the signal extracted by the signal processor 14 is supplied to the control circuit 18, whereby tracking control is effected, and a part of this signal is fed to the outside.

In this DAT 1, by connecting a digital-to-analogue (D/A)/analogue-to-digital (A/D) converting circuit to the output of the I/O circuit 13 and a predetermined control apparatus to the output of the control circuit 18, it is possible to record and/or reproduce, for example, an analogue audio signal.

In the present embodiment, however, an interface bus 3 is connected through a controller 2 as an external apparatus to the DAT 1. The bus 3 may be of the type which conforms, for example, to the SCSI (small computer system interface) standard (See NIKKEI ELECTRONICS, pages 102 to 107, published by Nihon Keizai Shinbunsha on 6 October 1986). A host computer 5 and a hard disc drive (HDD) 6 are connected to the bus 3 through a host adaptor 4.

In the controller 2, a protocol control circuit 21 is connected to the bus 3. Through the protocol control circuit 21, the data and the control signals are interchanged between a microcomputer 22 which controls the operation of the controller 2, a memory control or dynamic memory access (DMA) circuit 23 and the bus 3. The microcomputer 22 not only controls the operation of the controller 2, but also detects the address of the DMA circuit 23 and controls the operation of the DMA circuit 23. Also, data is interchanged between a buffer memory 24 and the interface bus 3 through the DMA circuit 23. Further, data is interchanged between the buffer memory 24 and the signal processor 14 in the DAT 1 via I/O circuits 25 and 13. In addition, the control signal is interchanged between the microcomputer 22 and the control circuit 18.

Accordingly, in this apparatus, data written in the HDD 6 is supplied through the bus 3 to the controller 2 in response to the transfer request from the controller 2 during recording, and is then written in the buffer memory 24 through the DMA circuit 23. The data written in the buffer memory 24 is read out through the I/O circuit 25, and then fed to the DAT 1. In the DAT 1, the data inputted to the I/O circuit 13 is regarded as being equivalent to that derived from the A/D converting circuit when an audio signal is recorded. Thus, this data is converted to a predetermined DAT format by the signal processor 14, and is thereby recorded on the tape 12 by the heads A and B.

Upon reproduction, the signal reproduced from the tape 12 by the heads A and B is reconverted by the signal processor 14, and thereby data corresponding to the audio signal is produced. This data is supplied through the I/O circuit 13 to the controller 2. In the controller 2, the data written in the buffer memory 24 through the I/O circuit 25 is read out through the DMA circuit 23, and is then written in the HDD 6 through the bus 3.

During the recording operation, the host computer 5 transmits data signals, for example, at a unit rate of 2^n (for example 512) bits to the DAT 1. Therefore, the data stored in the buffer memory 24 is supplied to the signal processor 14 such that an integral multiple of 2^n bits of data are recorded in one frame, which is made up of two oblique tracks formed during one rotation of the head drum 11 (see Japanese Patent Application No. 61/303080).

In this recording mode, the reading of the buffer memory 24 is controlled, for example, such that one to several frame portions of meaningless data are recorded every time a predetermined number of frames of data are recorded on the tape 12.

This recording mode will be described in detail with reference to Figure 2, which shows the entire data recorded at one time in the recording operation. First, a plurality of frames of amble signals (shown as hatched tracks) are recorded from the beginning (the left side in Figure 2) of the tape, and subsequently n frames of data signals are recorded after the amble signals. Then, for example, one frame of a meaningless dummy

signal (shown as hatched tracks) is recorded after the n frames of data signals. The n frames of data signals and one frame of dummy signal are repeatedly recorded. Finally, the remaining m (m is less than n) frames of data signals are recorded, and a plurality of the amble signals are thereafter recorded. Figure 3A shows in detail how the data signals are recorded between the dummy signals, wherein a period for recording n frames of data signals is provided after one frame of dummy signals (shown hatched) recorded by the heads A and B of the head drum 22, and another frame of dummy signals is provided after the data signal recording period. The desired data signals between the two dummy signal recording periods are extracted by the use of a timing signal such as, for example, a signal which is indicative of the frame number, or the like, contained in the data signal during reproduction.

When the data signals are re-recorded after they have been subjected to processing, such as editing or the like, under the condition that the rotary phase servo or the like of the head drum 11 is effected in advance of the tape location where the data signals to be re-recorded are recorded, the latter half of the dummy signals by the head B are recorded first, and the n frames of data signals are next recorded, and the dummy signal is only recorded by the head A, as shown in Figure 3B. Thus, the re-recording is ended.

With this process, a re-recording operation is accomplished as shown in Figure 3C. At the end portion of the re-recording, a portion of the track previously recorded by the head B is erased by the head A, which has a width wider than the track width. However, since the erased track has only dummy signals recorded thereon, no problem will occur.

As described above, the data signals recorded between the dummy signal frames can be arbitrarily re-recorded, so that editing, modification and so on of the recorded data signal can easily be carried out.

The number n of frames of data signals to be recorded between the dummy signal frames may be determined from the number of tracks to be recorded. Apart from this, when the data signals are repeatedly recorded upon the occurrence of recording errors, for example, as we have previously proposed in Japanese Patent Application No. 62/4434, the number n may be selected to be a substantial number of frames which have been recorded.

Generally, one frame of dummy signals is sufficient. However, if there is a fear that errors may be increased during re-recording while the data signals are repeatedly recorded as described above, a plurality of frames of dummy signals may be provided, taken in consideration of the above increased amount.

Moreover, in this case, the number of tracks maximally required to record substantially n frames of data signals is calculated from an assumed error occurring ratio or the like based on the recording medium, and then the number of tracks between the dummy frames may be set as this number. This method allows the recording position of the dummy signals always to be constant on the recording medium. Therefore, by determining the frame period in which the amble signals are recorded to be a period which is detectable by a high speed search operation or the like, a desired recording portion can be taken out from the tape on the basis of its distance after the detection.

In this embodiment, since one to several frames of meaningless data are recorded every time a predetermined number of frames of the digital signals are recorded, if the meaningless data frames are also recorded upon the re-recording of the data signals, the re-recording can be smoothly carried out without destroying any part of the required data signals. Thus, it is possible to provide a satisfactory data recorder using a DAT.

Next, a second embodiment of the invention will be described with reference to Figure 4. Parts in Figure 4 corresponding to those in Figure 1 will not be described again.

As in the embodiment of Figure 1, the controller 2 of Figure 4 is provided with the protocol control circuit 21 which is connected to the bus 3. The microcomputer 22 for controlling operations of the controller 2 and the DMA 23 communicate data and control signals with the bus 3 through the protocol control circuit 21. The microcomputer 22 detects conditions of the DMA 23 and controls its operations, while the buffer memory 24 communicates with the bus 3 through the DMA 23.

In this embodiment, however, the buffer memory 24 is provided with an error correcting code (ECC) generating circuit 26 which generates an error correcting code for the data which is stored in the buffer memory 24. This ECC is also stored in a predetermined area of the buffer memory 24.

The buffer memory 24 communicates with the processor 14 of the DAT 1 through the I/O circuits 13 and 25. Also, the microcomputer 22 communicates with the system control circuit 18 of the DAT 1 as in the embodiment of Figure 1.

With the construction shown in Figure 4 and described above, the data stored in the HDD 6 is supplied to the controller 2 through the bus 3 in response to a transmission request made by the controller 2, and is stored in the buffer memory 24 through the DMA 23 upon recording. The ECC generating circuit 26, under the control of the microcomputer 22, generates the ECC for the data stored in the buffer memory 24. The data including the ECC is next read out of the buffer memory 24 and supplied to the DAT 1 through the I/O circuit 25.

In the DAT 1, the data supplied to the I/O circuit 13 is processed by the signal processor 14 in the same manner as audio data from an A/D converter, and is converted to the predetermined DAT format and is then recorded on the tape 12 by the heads A and B.

The DAT format is such that 5760 bytes of original data can be recorded in one frame, which is made up of two oblique tracks formed by one rotation of the head drum 11. For the case in which one unit is formed of twelve frames, eleven frames are each used to record 5760 bytes of data therein, while the remaining one frame is used to record only 2176 bytes of data. The remaining bytes are of invalid data. In this manner, 65536

bytes (64 Kbytes) can be recorded in the above-mentioned one unit (twelve frames).

When 64 Kbytes of data have been stored in the buffer memory 24, the ECC generating circuit 26 generates the ECC. For this ECC, a Reed-Solomon code is employed. The twelve frames of data are provided, for example, with a two-frame portion of the ECC. The generated ECC is stored in a predetermined area of the buffer memory 24.

During recording, the buffer memory 24 is controlled by the microcomputer 22 in such a manner that first one frame portion of the ECC, then twelve frame portions of data signals, and finally one frame portion of the ECC are read out of the buffer memory 24 to the I/O devices 25 and 13, and are recorded by the heads A and B.

Thus, a recording pattern made on the tape 12 is as shown in Figure 5A, wherein one frame of the ECC signal is located ahead of twelve subsequent frames of data signals (a part of which is omitted in the drawing) and another frame of the ECC signal, which are respectively recorded by the heads A and B mounted on the head drum 11. Upon reproduction, the desired data signals located between the ECC frames are taken out by the use of a timing signal such as a signal indicative of the frame number or the like contained in the data signals.

Assume now that the data signals are to be re-recorded again after processing, such as editing, has been effected thereon, under the condition that the head drum 11 is servo-controlled by, for example, a rotating phase servo, from a tape location before where the data signals which are to be re-recorded are recorded. Under such conditions, the latter half of the ECC signal in the ECC frames originally recorded by the head B is first recorded, twelve frames of the data signals are next recorded, and only the ECC signal originally recorded by the head A is recorded as shown in Figure 5B. Then, the re-recording is ended.

With the process described above, the re-recording is accomplished as shown in Figure 5C. It can be seen from Figure 5C that one frame portion of the ECC signal has been deleted by the re-recording. Although upon reproduction, the error correcting ability is somewhat degraded by this deletion of the ECC signal, since the data signals are preserved, no problem will occur in ordinary use.

As described above, the second embodiment allows arbitrary recording of the data signals located between the ECC frames, so that editing, modifying and so on can easily be carried out on the recorded data signals.

Incidentally, when k frames of ECC are provided for the data signals, it is possible to correct errors occurring in up to k frames of the data signals. Therefore, when a read-after-write head is used to check errors in recorded data signals, the data signals can be recorded while errors occurring in up to k frames are ignored. Therefore, a procedure for repeatedly recording the data signals, for example, when errors occur during recording, can be substantially simplified.

If errors occur in more than k frames of the data signals, the entire block of the data signals between the ECC frames may be repeatedly recorded. Since the data signals are divided into sufficiently small blocks by the ECC frames, it is easy to record the data signal block repeatedly.

The value k should be replaced by k-1 upon the first re-recording.

Further, an identification (ID) code, indicative of the number of re-recording may be inserted, for example, in each frame, so as to prevent erroneous detection of an ECC frame which remains unerased in the preceding re-recording. With such an ID code, it is possible to ignore frames except for the frame that has the same value as the number of the re-recording.

Also, by using a data sequence which can be interleaved between the respective tracks as the data used for generating the ECC, it is possible to improve the error correcting ability for errors caused by horizontal scratches or the like on the tape.

Moreover, in the second embodiment, it is possible to provide a sufficient number of ECC frames, such that the ECCs are recorded in all of the provided ECC frames for a high grade apparatus, or the ECCs are recorded only in a portion of the ECC frames and meaningless data is recorded in the remaining portion for a low grade apparatus.

With the second embodiment, as described above, during recording, one to several frames of the ECC are recorded in place of the dummy signals every time a predetermined number of frames of the data signals are recorded, so that the error correcting ability can be largely improved. The ECC frames are also recorded upon re-recording, so that necessary data signals can be re-recorded smoothly without being destroyed, thereby to provide a satisfactory data recorded which employs a DAT.

Reference is next made to how, in actual practice, the ECC is recorded in the corresponding frames in the recording operation, by way of example.

The DAT format is, as shown in Figure 6, such that data is interleaved in one frame which is made up of two oblique tracks formed by one rotation of the drum 11, in a manner such that even numbered data of the left channel is recorded in the former half of one track (plus azimuth) of one frame, and odd-numbered data of the right channel is recorded in the latter half of the same track, while even-numbered data of the right channel is recorded in the former half of the other track (minus azimuth) of the same frame and odd-numbered data of the left channel is recorded in the latter half of the same track. Reference letter "C" in the centre of each track in Figure 6 represents the ECC added to each track by the DAT 1. In generating the ECC, 2n'th (even-numbered) data and (2n+1)'th (odd-numbered) data of each frame are taken out to form a data sequence, thereby to generate the ECC to be recorded in the ECC frame for the interleaved data sequence on the tape 12.

An error correcting code generating matrix is arranged for the data sequence, for example, as follows:

1	...	1	1	1	1	1	1
α^{254}	...	α^{5}	α^{4}	α^{3}	α^{2}	α^{1}	1
α^{508}	...	α^{10}	α^{8}	α^{6}	α^{4}	α^{2}	1
α^{762}	...	α^{15}	α^{12}	α^{9}	α^{6}	α^{3}	1
Data section				Parity section			

A syndrome generating circuit is formed for the matrix thus generated, for example, as shown in Figure 7. Specifically, a data signal fed to a terminal 31 on the left of the drawing is supplied to adder circuits 32a to 32d. The output signals from the adder circuits 32a to 32d are respectively supplied to syndrome registers 34a to 34d directly and through coefficient circuits 33b to 33d respectively having coefficients of α, α^2 and α^3. The signals from the syndrome registers 34a to 34d are respectively fed back to the adder circuits 32a to 32d. Thus, syndromes are generated in the registers 34a to 34d by the feedback which are effected every time the data signal is supplied to the adder circuits 32a to 32d.

Therefore, every time the data signal is fed to the terminal 31, calculation is effected from the right side of the data section of the above matrix. Generally, at the time, for example, where 251 symbols of data have been supplied, the syndromes are generated from the registers 34a to 34d. The syndromes thus generated are supplied to a calculating circuit 35, which corresponds to the parity section of the above matrix, to generate a 4-symbol ECC. If the data sequence is terminated while the calculation is progressing, the registers 34a to 34d respectively generate the syndromes equivalent to the fact that zero is supplied to all the elements of the syndromes located on the left side from the point the calculation based on the data sequence has been effected. Then, at this time, the registers 34a to 34d are made inoperative, and the respective contents thereof are supplied to the calculating circuit 35, thereby to generate the ECC, for the data which has been supplied to the syndrome generating circuit up to that time.

By this processing, the ECC can be smoothly generated and added to an arbitrarily variable length of data sequence. In this case, the above-mentioned syndrome generating circuit is realized in practice by software of a microcomputer or the like. The required hardware is solely memory areas corresponding to the syndrome registers 34a to 34d, so that the apparatus can be realized by a simple construction. That is, the memory capacity of each of the registers 34a to 34d is four times the data amount for one track, so that it will be understood that the syndrome generating circuit can be easily constructed with an extremely small memory capacity, and a properly programmed microcomputer.

Referring now to Figure 12, a flow chart for such a syndrome generating program is illustrated. The program starts at step SP1 and the data signal is input at step SP2. At step SP3, the input data signal is added to the stored data signal in memory M1 (within the buffer memory 24) and the added data signal is stored in memory area M2 of the buffer memory 24.

The input data signal, at step SP4, is added to the stored data signal in the memory area M2. The added data signal is multiplied by a coefficient α. The multiplied data signal is stored in the memory area M2. In step SP5, the input data signal is added to the stored data signal in memory area M3 of the buffer memory 24, the added data signal is multiplied by a coefficient α^2. The multiplied data signal is stored in the memory area M3.

Next, the input data signal is added to the stored data signal in memory area M4 of the buffer memory 24. The added data signal is multiplied by a coefficient α^3. The multiplied data signal is stored in the memory area M4 at step SP6. At step SP7 it is determined whether or not the input data signal is finished. If the answer is no, the process returns to step SP2. If the answer is yes, the process goes to step SP8 where four ECCs are generated from the stored data signals in the memory areas M1, M2, M3 and M4 by matrix calculations. This ends the process.

The generated ECC is supplied to the DAT 1 subsequent to the data signals, so as smoothly to record an arbitrarily variable length of the data signals, thereby rendering it possible to provide a satisfactory data recorder using the DAT.

In the above described embodiment, since two symbols are taken out from each frame of the data sequence for generating the ECC, the generated 4-symbol ECC can be recorded in two frames (four tracks).

If, as a particular example, the ECC is assumed to be formed of two symbols, the following matrix, for example, may be used.

1	...	1	1	1	1
α^{254}	...	α^{2}	α	0	1

With this matrix, the calculating circuit 35 becomes unnecessary.

Next, an explanation will be given of how error correcting processing is carried out during reproduction by the aforementioned apparatus, with reference to Figures 8A to 8E.

First, the data signals and the ECC are reproduced as shown in Figure 8A. If the DAT 1 detects that there is a frame whose error cannot be corrected as shown in Figure 8B, a condition where the data has been directly outputted at first is halted as shown in Figure 8C. However, at this time the data signals are continuously supplied to the syndrome generating circuit, so that the syndrome generating circuit generates data for correcting errors in the erroneous frame at the time the reproduction of the ECC has been terminated. From this condition, the DAT 1 is instructed to rewind the tape 12 as shown in Figure 8D. Then, as shown in Figure 8E the DAT 1 again starts the reproduction of the data signals from the beginning thereof, in which the error correcting data generated by the syndrome generating circuit is inserted for the detected erroneous frame, and then all the data signals are reproduced.

When no error is found in the data frames as usual, the data signals are reproduced as they are and outputted to the bus 3 without any other processing. The above described processing is effected only when errors are found in the data frames, so that the data signals as a whole can be quite rapidly reproduced.

The above described error correction can be effected with only a small capacity of the memory area corresponding to the syndrome registers 34a to 34d by using the data signals again reproduced from the DAT 1, without the necessity of providing a large capacity buffer memory for storing all data in the data section of the foregoing matrix.

The error correction as described above requires, upon reproduction, detecting at least the frame number of the ECC, and discriminating whether the frame contains the data signals or the ECC. Therefore, a signal area is reserved in the DAT format for such detection and discrimination. This DAT format, in accordance with which the data signals are recorded on the tape 12, will be explained with reference to Figure 9.

As can be seen from Figure 9, one frame is made up of two tracks Ta and Tb formed by the heads A and B. Each of the tracks Ta and Tb has a length corresponding to the rotation of each of the respective heads through an angle of 90° and is partitioned from its lower end (that is, from right to left in the figure) into 5.051° of a margin area, 0.918° of a preamble area for the phase locked loop (PLL) of the sub-code, 3.673° of a first sub-code, 0.459° of a postamble area, 1.378° of an interblock gap area, 2.296° of a tracking (ATF) signal area, 1.378° of an interblock gap area, 0.918° of a preamble area for the PLL of data, 58.776° of data area, 1.378° of an interblock gap area, 2.296° of an AFT signal area, 1.378° of an interblock gap area, 0.918° of a preamble area for the PLL of the sub-code, 3.673° of a second sub-code area, 0.459° of the postamble area, and 5.051° of the margin area. It should be noted that the scale of the respective areas in Figure 9 is not exact.

Data fed to the DAT 1 at the I/O circuit 13 is supplied to the signal processor 14 which adds predetermined error detecting and correcting codes and so on to the data, and then inserts it into the data areas of the tracks Ta and Tb in accordance with a predetermined interleaving relationship.

As illustrated in Figure 11A, the data area comprises an 8-bit synchronizing section at its starting portion and subsequently totals 16 bits of ID section formed of W1 and W2. The ID section is divided into eight ID areas of two bits. The first ID area (ID-0) is assigned to a format ID and is set to "01" for a data specification, for example. The next ID area (ID-1) is assigned to a sub-category ID and is set to "00" for a computer peripheral device, for example. The next ID area (ID-2) is assigned to a frame size ID and is set to "00" when the recording capacity of the frame is 5760 bytes and "01" when the recording capacity of the frame is 5292 bytes, for example. The ID area (ID-3) is assigned to a track pitch ID and is set to "00" when the track pitch is 13.6 μm and "01" when the track pitch is 20.4 μm, for example.

As illustrated in Figure 11B, the sub-code area also comprises an ID section formed of W1 and W2. The first bit of W1 is assigned to a code indicative of validity (set to "1") or invalidity (set to "0") of data. The next three bits of W1 are a code indicative of a location of an area including a frame. Specifically, this code is set to "000" when the area is located at a read-in area, that is, the beginning of a tape, "001" when in the data area, "010" when in a read-out area, that is, the end of a data recording area, "011" when at the end of the medium, that is, the end of the tape. The remaining four bits of W1 is assigned to a code indicative of an ordinary frame (set to "0**0", an amble frame used for synchronization or the like (set to "0**1", a frame other than a file mark (set to "000**"), a first file mark (set to "001**"), a second file mark (set to "010**"), or a third file mark (set to "011**"). On the other hand, W2 has its first bit set to "1", the next three bits set to "000" which indicates that the following sub-code is a pack format, as will be later referred to, and the last four bits set to a value indicative of a block address.

A variety of determinations can be carried out by means of the above-mentioned information when the DAT is used as a data recorder.

The first and second sub-code areas respectively have a capacity capable of recording 2048 bits of data. According to the DAT format for audio signals, 2048 bits are divided into 64-bit packs, each of which is used to record therein information such as the time code of the recorded signal, and the recording date.

It is possible to use the packs for recording information on the data recorder, whereby a variety of control operations can be effected by the use of a pair of the packs. Figure 10 shows formats of the packs for the control operations. As is apparent from the tables in Figure 10, each pack of 64 bits is divided into eight words each comprising eight bits. The upper four bits of the top or first word of each pack is assigned to an ITEM area which, common to the recording format for audio signals, shows the contents of the pack by its four binary codes. Nine of the sixteen combinations made by four bits have already been assigned for audio signal

recording, so that the indication of the data recorder is arbitrarily selected from the remaining seven combinations, for example, the ITEM area of the first pack of the two packs in use is set to "0010" and that of the second pack to "0001".

A total 20-bit area made up of the lower four bits of the first word and the second and third words of the first pack is assigned to a logical frame number (LFNO) area in which is recorded, for example, a binary-code combination indicative of the serial number of a valid frame from the head of the tape.

A total 16-bit area made up of the fourth and fifth words of the first pack is assigned to a save set number (SSNO) area in which is recorded, for example, a binary-code combination indicating how many times the back-up has been carried out from the initial use of the apparatus.

An area made up of the sixth and seventh words of the first pack is assigned to a file number (FNO) area in which is recorded a binary-code combination indicative of the serial number of a file within all the files of data backed up (saved) at one time.

The eighth word of the first pack is assigned to a parity for the first to seventh words.

A total 20-bit area made up of the lower four bits of the first word and the second and third words of the second pack is assigned to indicate frame conditions. Specifically, the upper two bits of the upper four bits of the first words are set to a code indicative of the aforementioned amble area (set to "00"), data area (set to "01"), read-out area (set to "10"), or end of medium (set to "11"), while the lower two bits of the same are set to a code indicative of an ordinary frame (set to "0*"), a file mark frame (set to "1*"), valid data (set to "*0"), or invalid data (set to "*1"). The lower four bits of the second word is set to the number (PFL) of frames of the ECC in a binary code. The third word is set to the total number (ECFL) of data signal frames and ECC frames in a binary code, all the bits of which are set to "0" if the number of frames is indefinite.

The fourth word is assigned to the number (EFNO) of frames to which the ECC has been added. When the first or most significant bit thereof is set to "0", it indicates that the frame concerned is a data signal frame, and the subsequent seven bits thereof are set to a binary-code combination indicative of the serial number of the data signal frame. On the contrary, if the first bit is set to "1", it indicates that the frame concerned is an ECC frame, and the subsequent seven bits thereof are set to a binary-code combination indicative of the serial number of the ECC frame.

The first or most significant bit of the fifth word is a flag (F1) which indicates whether signals of the sub-code area are recorded also in the data area (set to "1") or not (set to "0"). The next two bits of the fifth word are set to a binary-code combination indicative of a file mark order (#FM). The lower five bits of the fifth word and the sixth word are assigned to indicate the number (EBL) area of bytes of valid data in a frame and set to a binary-code combination indicating the number of bytes.

The upper four bits of the second word and the seventh word are reserved as extended bits and are all set to "0" for the moment. The eighth word is assigned to a parity for the first to seventh words.

Thus, the data signals can be quite smoothly reproduced by identifying these ID codes and so on as described above.

It is therefore possible to use the DAT as a data recorder, wherein the head drum 11 is rotated, for example, at 2000 rpm, so that data is quite rapidly recorded at a rate of 192,000 bytes per second and consequently consumption of the recording medium can be substantially reduced. Moreover, the data can be smoothly recorded with the ECC added thereto, which permits a satisfactory data recording.

With the second embodiment as described above, since the frame of ECC added to data and so on are included in the DAT format, it is possible to generate the ECC for an arbitrary length of data sequence and thereby smoothly record the arbitrary length of the data sequence, whereby a satisfactory data recorder which employs the DAT can be provided.

Claims

1. An apparatus for recording digital data on a recording medium (12), the apparatus comprising:
recording means (1) for recording an inputted digital signal in one frame, which is made up of two oblique tracks formed by rotary heads;
characterized by:
control means (2) for dividing said digital data into predetermined frame portions, and supplying the divided digital data to said recording means (1).

2. An apparatus according to claim 1 wherein said control means (2) comprise means (22 to 25) for supplying a predetermined frame portion of a dummy signal as a digital signal to said recording means (1) at each predetermined frame portion.

3. An apparatus according to claim 1 wherein said control means (2) comprise means (26) for generating a predetermined frame portion of an error correcting code for said predetermined frame portion of the digital data at each predetermined frame portion; and means (22 to 25) for supplying said error correcting code as a digital signal to said recording means (1) at each predetermined frame portion.

4. An apparatus according to claim 3 further comprising means (22 to 25) for recording separate discriminating signals for discriminating each frame in which said digital data information is recorded and

each frame in which said error correcting code is recorded.

5. An apparatus according to claim 4 wherein each of said discriminating signals is recorded in a sub-area of the recording medium (12) different from a main area of the recording medium (12) in which said digital data information is recorded.

6. An apparatus according to claim 4 further comprising:
reproducing means (17) for reproducing digital signals and said discriminating signal recorded in the oblique tracks by rotary heads (A,B);
first error correcting means for correcting errors in the reproduced digital signals;
means (34) for generating a syndrome for correcting errors on the basis of said reproduced discriminating signal;
means for halting the output of the reproduced digital signals when an error which cannot be corrected by said first error correcting means occurs in said reproduced digital signal;
means for reproducing recorded digital signals again after said syndrome has been generated; and
outputting means (35) for correcting said error occurring in said digital signal by said syndrome and for outputting said digital signal free of said error as digital data.

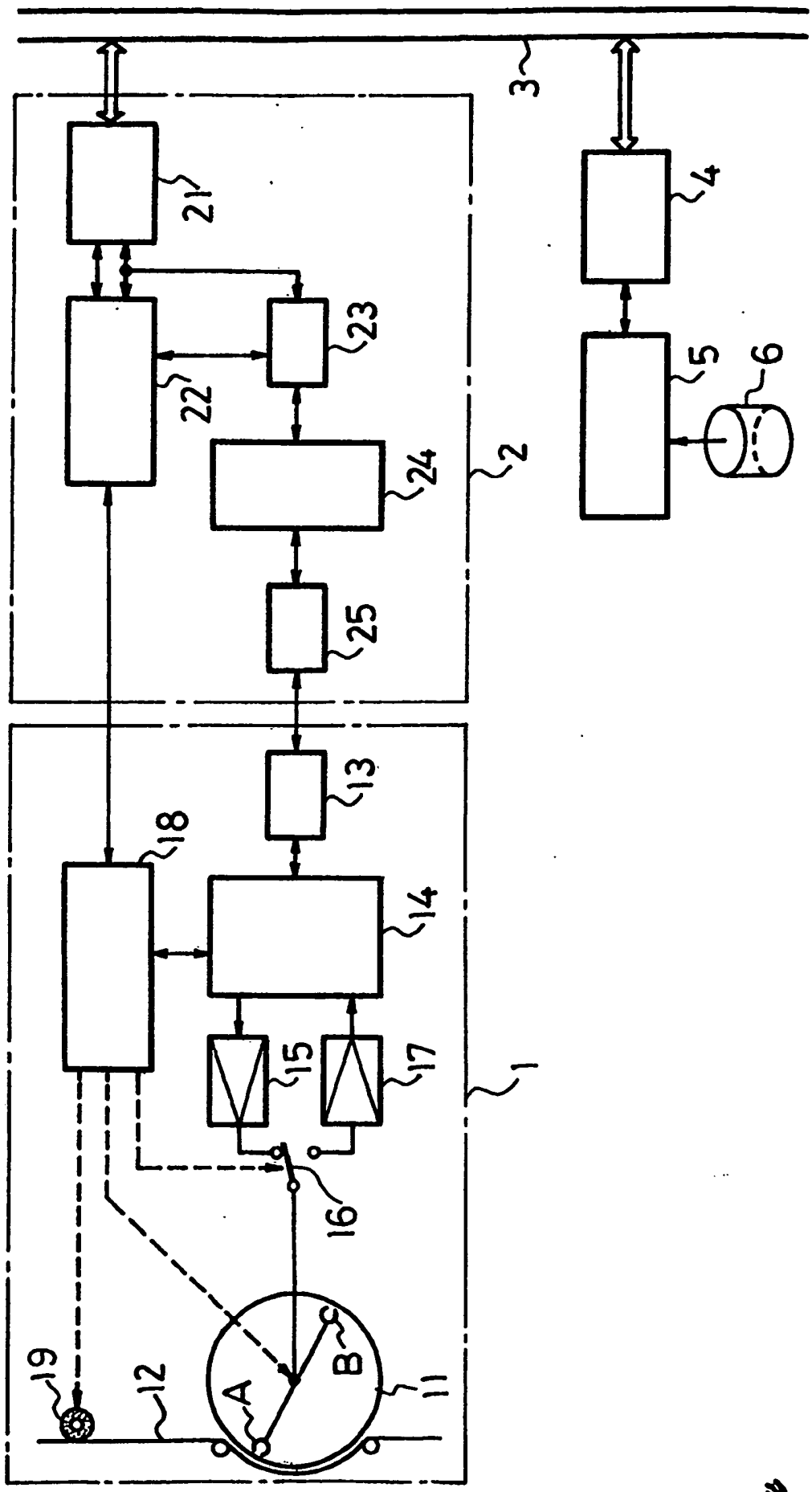
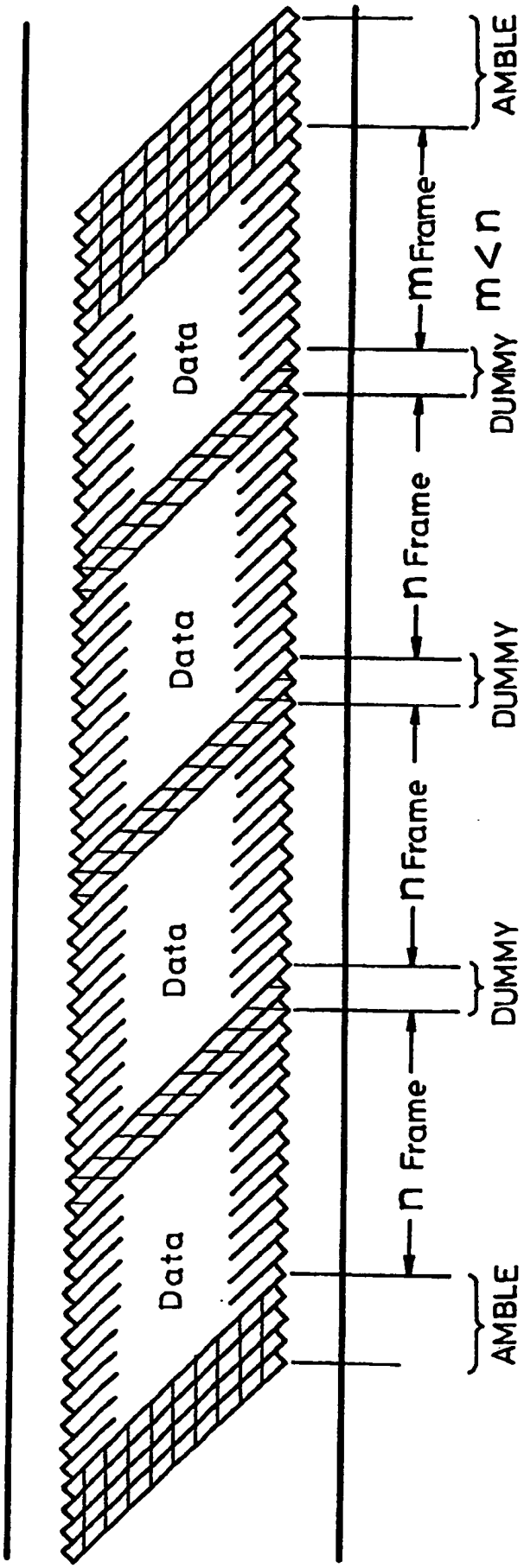


FIG. 1

FIG. 2


AMBLE
m Frame
m < n
DUMMY
Data
n Frame
DUMMY
Data
n Frame
DUMMY
Data
n Frame
AMBLE
Data

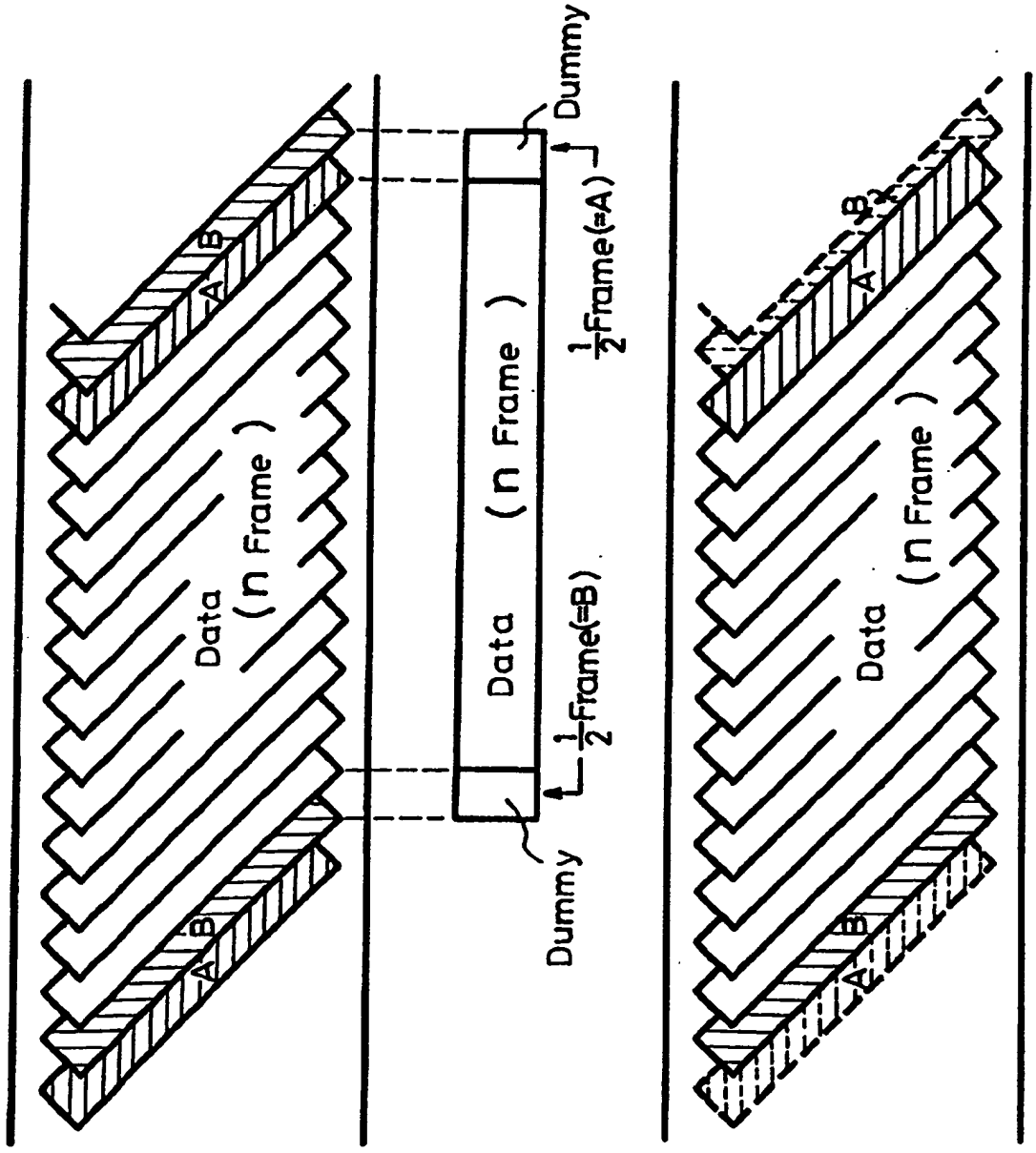


FIG. 3A

FIG. 3B

FIG. 3C

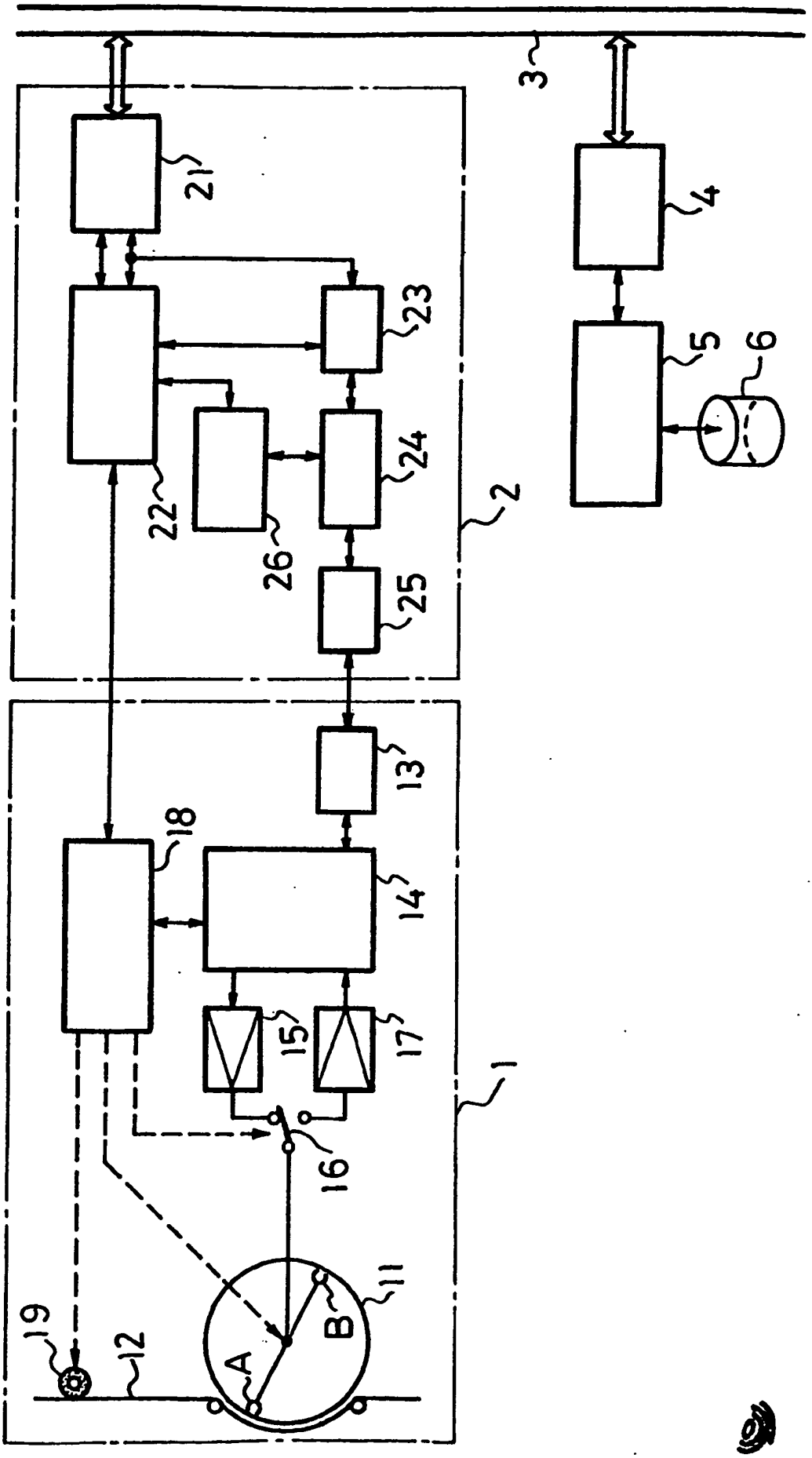


FIG. 4

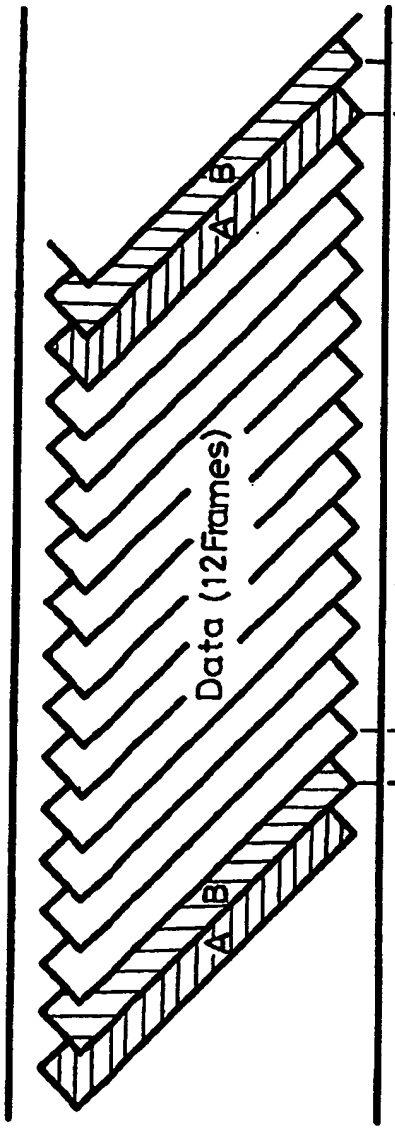


FIG. 5A

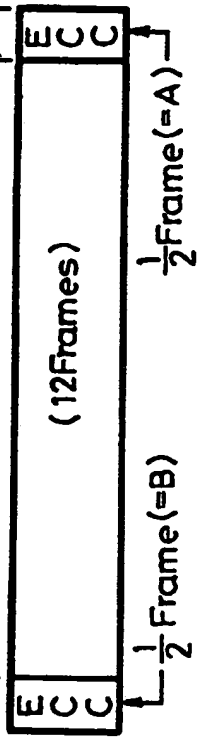


FIG. 5B

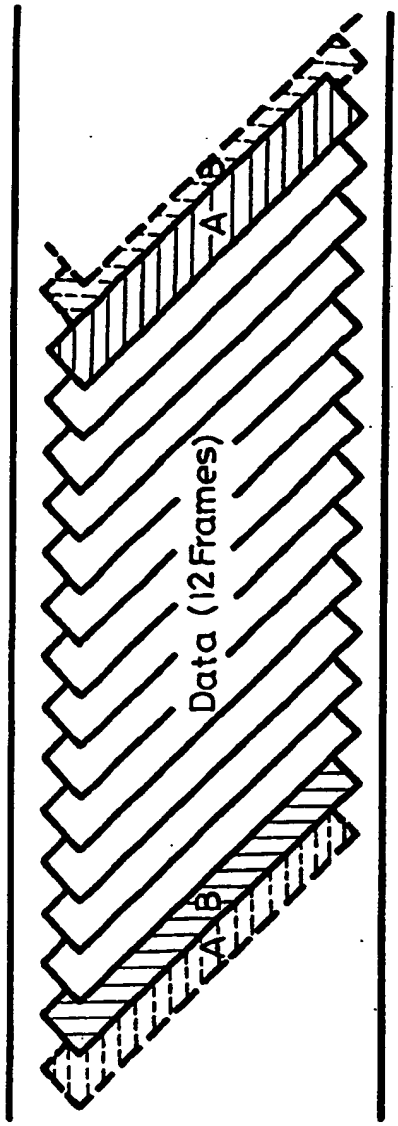


FIG. 5C

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FIG. 6

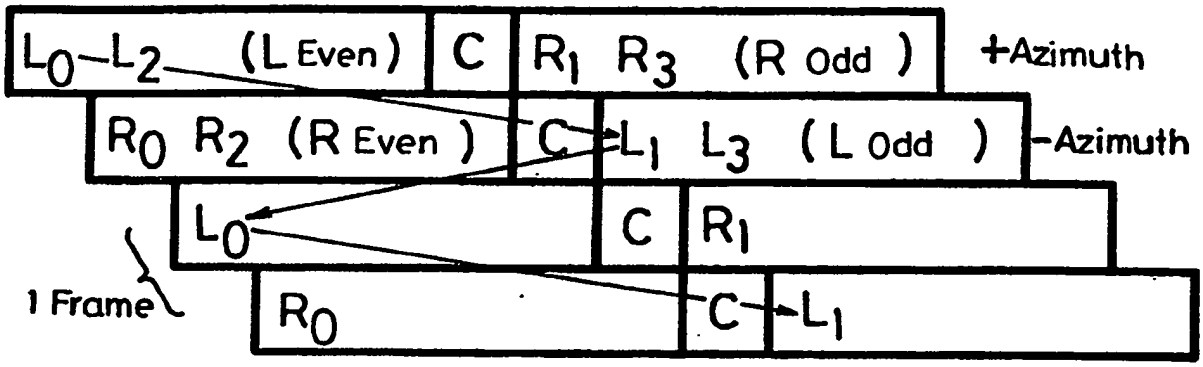


FIG. 7

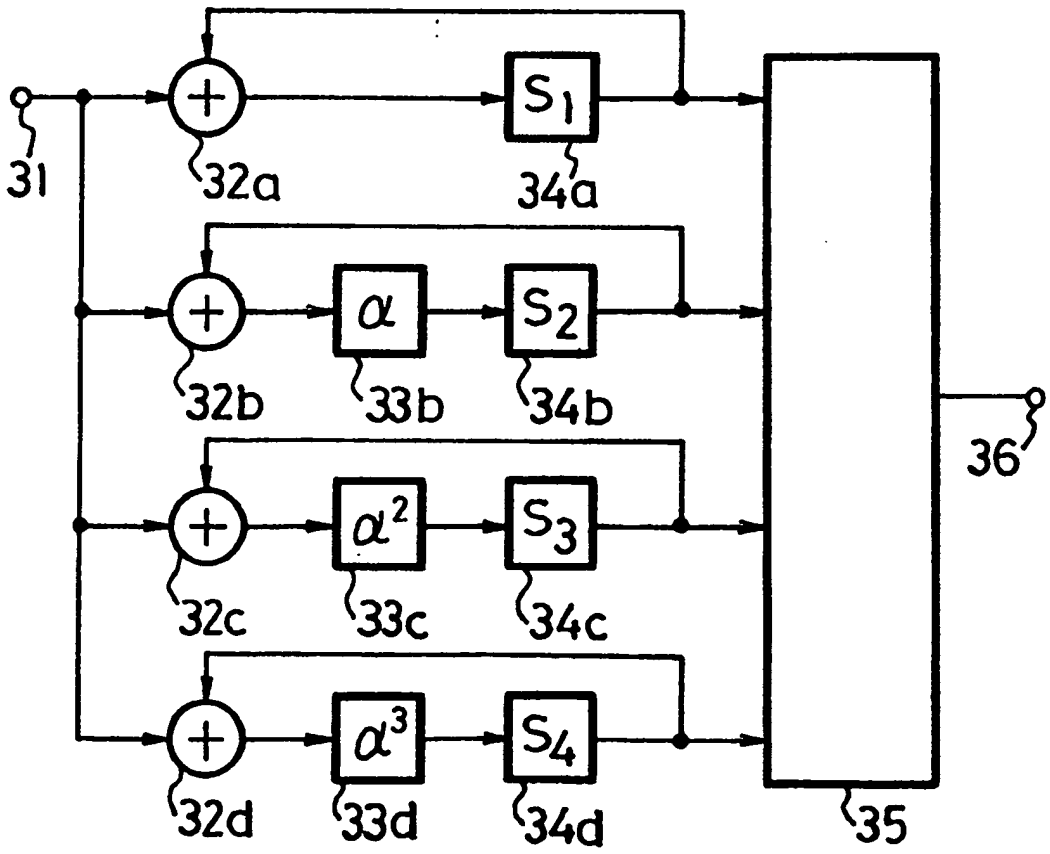


FIG. 8A

FIG. 8B

FIG. 8C

FIG. 8D

FIG. 8E

FIG. 9

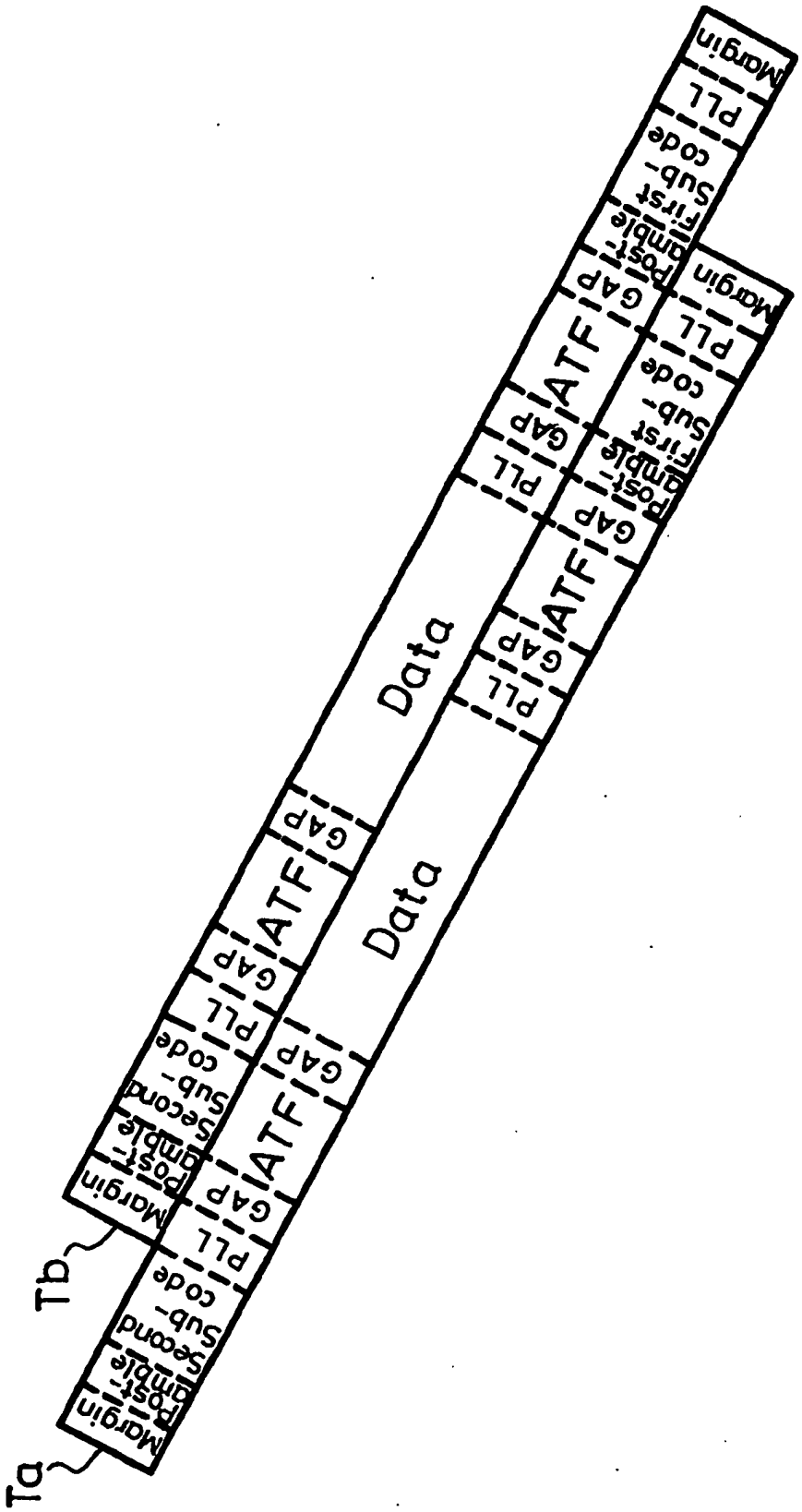
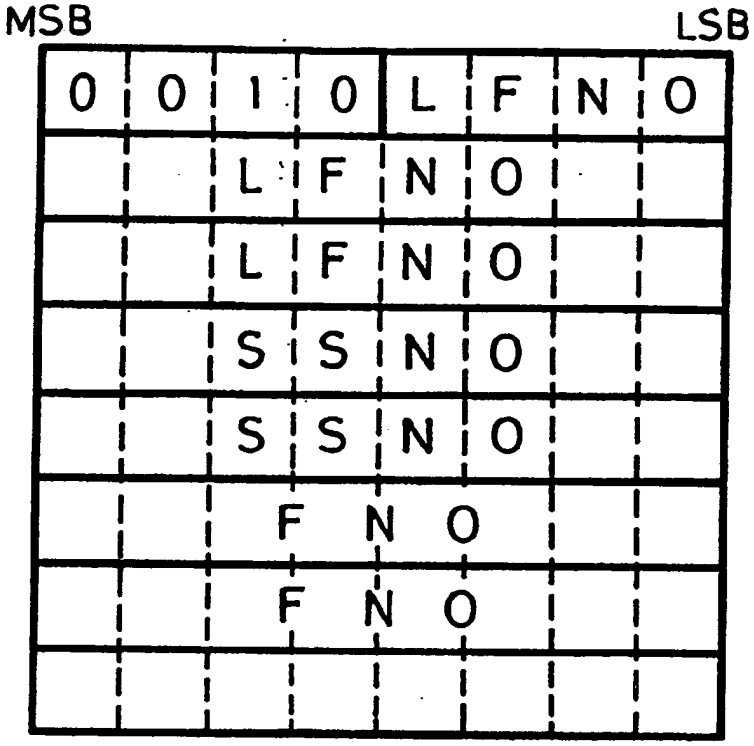

Ta
Tb
Margin
Post-amble
Second Sub-code
PLL
GAP
ATF
Data
First Sub-code

FIG. 10


MSB
LSB
0 0 1 0 L F N O
L F N O
L F N O
S S N O
S S N O
F N O
F N O

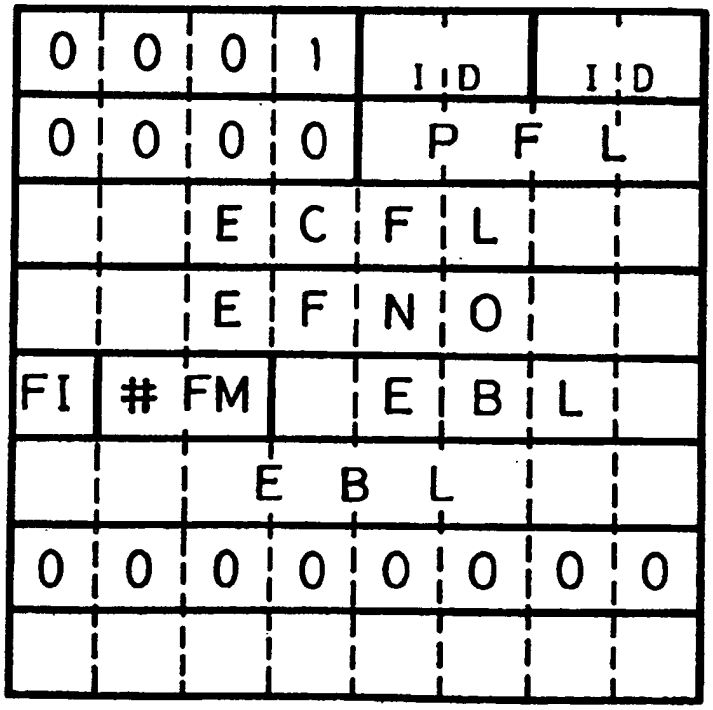

0 0 0 1 I D I D
0 0 0 0 P F L
E C F L
E F N O
FI # FM E B L
E B L
0 0 0 0 0 0 0 0

FIG. 11A

W1 (DATA-ID) 8 bit			W2 (Block Address) 8 bit
ID-0	ID-1	Frame Address	0 X X X X 0 0 0
Optional Code			0 ↑ 0 0 1
ID-2	ID-3	Frame Address	0 ↑ 0 1 0
Optional Code			0 ↑ 0 1 1
ID-4	ID-5	Frame Address	0 ↑ 1 0 0
Optional Code			0 ↑ 1 0 1
ID-6	ID-7	Frame Address	0 ↑ 1 1 0
Optional Code			0 ↑ 1 1 1

FIG. 11B

SUB-CODE ID				
W1 (8 bit)			W2 (8 bit)	
Validity	Location	Frame Filemark		Block Address
0	0 0 0	0 * * 0	1 0 0 0	X X X X

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FIG. 12